

CLAIMSWhat is claimed is:

1. A method of designing a programmable logic device comprising the steps of:

identifying a cost function that penalizes floorplans of a circuit design that do not fit on the programmable logic device;

defining modules comprising components of a same type;

determining a set of shapes associated with at least one module; and

annealing the circuit design to determine a floorplan using the cost function and the set of shapes for the at least one module.

2. The method of claim 1, said defining step further comprising splitting modules into sub-modules, wherein at least one of the sub-modules consists of components of a same type.

3. The method of claim 1, said annealing step further comprising assigning modules to a particular one of the set of shapes associated with that module.

4. The method of claim 3, said annealing step further comprising assigning modules and assigned shapes to locations on the programmable logic device.

5. The method of claim 4, said annealing step further comprising at least one of swapping locations of components of a same type that have associated grid sites, swapping two modules in a sequence pair, and switching the shape of a module from one shape in the set of shapes associated with that module to another.

6. The method of claim 4, said annealing step further comprising using bipartite matching of individual components.

7. The method of claim 4, further comprising:
identifying modules that share a timing critical path;
and
moving identified modules closer to one another.
8. The method of claim 1, wherein the programmable logic device is a Field Programmable Gate Array.
9. The method of claim 1, wherein each shape of a set of shapes associated with a module has a minimum width and height of at least a width and height of a largest relatively placed module to be placed within that module.
10. The method of claim 1, further comprising:
generating a flat placement flow for the circuit design;
and
comparing the annealed circuit design with the flat placement flow to determine a measure of quality for the determined floorplan.
11. A system for designing a programmable logic device comprising:
means for identifying a cost function that penalizes floorplans of a circuit design that do not fit on the programmable logic device;
means for defining modules comprising components of a same type;
means for determining a set of shapes associated with at least one module; and
means for annealing the circuit design to determine a floorplan using the cost function and the set of shapes for the at least one module.
12. The system of claim 11, said means for defining further comprising means for splitting modules into sub-modules,

wherein at least one of the sub-modules consists of components of a same type.

13. The system of claim 11, said means for annealing further comprising means for assigning modules to a particular one of the set of shapes associated with that module.

14. The system of claim 13, said means for annealing further comprising means for assigning modules and assigned shapes to locations on the physical device.

15. The system of claim 14, said means for annealing further comprising means for performing at least one of swapping locations of components of a same type that have associated grid sites, swapping two modules in a sequence pair, and switching the shape of a module from one shape in the set of shapes associated with that module to another.

16. The system of claim 14, wherein said means for annealing use bipartite matching of individual components.

17. The system of claim 14, further comprising:
 means for identifying modules that share a timing critical path; and
 means for moving identified modules closer to one another.

18. The system of claim 11, wherein the programmable logic device is a Field Programmable Gate Array.

19. The system of claim 11, wherein each shape of a set of shapes associated with a module has a minimum width and height of at least a width and height of a largest relatively placed module to be placed within that module.

20. The system of claim 11, further comprising:

means for generating a flat placement flow for the circuit design; and

means for comparing the annealed circuit design with the flat placement flow to determine a measure of quality for the determined floorplan.

21. A machine readable storage, having stored thereon a computer program having a plurality of code sections executable by a machine for causing the machine to perform the steps of:

identifying a cost function that penalizes floorplans of a circuit design that do not fit on a programmable logic device;

defining modules comprising components of a same type;

determining a set of shapes associated with at least one module; and

annealing the circuit design to determine a floorplan using the cost function and the set of shapes for the at least one module.

22. The machine readable storage of claim 21, said defining step further comprising splitting modules into sub-modules, wherein at least one of the sub-modules consists of components of a same type.

23. The machine readable storage of claim 21, said annealing step further comprising assigning modules to a particular one of the set of shapes associated with that module.

24. The machine readable storage of claim 23, said annealing step further comprising assigning modules and assigned shapes to locations on the physical device.

25. The machine readable storage of claim 24, said annealing step further comprising at least one of swapping locations of components of a same type that have associated grid sites,

swapping two modules in a sequence pair, and switching the shape of a module from one shape in the set of shapes associated with that module to another.

26. The machine readable storage of claim 24, said annealing step further comprising using bipartite matching of individual components.

27. The machine readable storage of claim 24, further comprising:

identifying modules that share a timing critical path;
and
moving identified modules closer to one another.

28. The machine readable storage of claim 21, wherein the programmable logic device is a Field Programmable Gate Array.

29. The machine readable storage of claim 21, wherein each shape of a set of shapes associated with a module has a minimum width and height of at least a width and height of a largest relatively placed module to be placed within that module.

30. The machine readable storage of claim 21, further comprising:

generating a flat placement flow for the circuit design;
and
comparing the annealed circuit design with the flat placement flow to determine a measure of quality for the determined floorplan.